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REMARKS

This Preliminary Amendment amends the above-identified Utility Patent Application filed herewith. With this Amendment, claims 2-12 and 14, 15 and 17 were amended. Claims 18-20 are added and thus claims 1-20 remain pending for consideration and allowance.

Specification

Submitted with this Preliminary Amendment is a substitute specification correcting informalities, clarity and context to the application originally filed (MPEP 608.01(q)). This substitute specification includes no new matter. A marked-up version of the substitute specification showing all of the changes to the specification is provided. Applicants respectfully request entry of this substitute specification.

Respectfully submitted,

Josef Hölze,

By his attorneys,

Dated: July 6, 2004
PPK:jan

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 6th day of July, 2004.

By
Name: Paul P. Kempf

STORAGE CAPACITOR WITH HIGH MEMORY CAPACITY AND LOW SURFACE AREA

Cross-Reference to Related Applications

This Utility Patent Application claims priority to German Patent Application No. DE 103 03 738.1, filed on January 30, 2003, which is incorporated herein by reference.

Background

The present invention relates to a storage capacitor, in particular one that can be used for 1T-, 2T- and 3T-memory cells in, for example, system-on-chip applications, which provides high capacity with low surface area usage.

In dynamic RAM memories, the information to be stored by a memory cell is generally held on a capacitor known as a storage capacitor. In system-on-chip applications in a pure logic technology, storage capacitors are often created by means of the gate capacity of an MOS transistor (e.g. a MoSyS-1T-SRAM, a 1T-cell of a static random access memory from MoSys Inc.) or by means of connection in parallel of gate and diffusion capacity (e.g. IFX-2T concept, a 2T-cell concept from Infineon).

Because of the leakage currents, a storage capacitor slowly loses its charge, which can lead to the loss of the information stored on the capacitor. In order to counter this, in microelectronic circuits the charge of all storage capacitors is refreshed again at certain intervals, so that the information is retained. This interval depends, amongst other things, on the size of the memory capacity.

As a result of increasing integration, the leakage currents in the abovementioned system-on-chip applications are becoming ever greater and new leakage current sources such as the gate leakage currents are arising due to the increasingly thin oxide coatings. The total memory capacity is also becoming smaller.

Summary

One embodiment of the invention provides a storage capacitor with high memory capacity low surface area usage, which in particular in a pure logic technology can be created without additional, and thus more expensive, process steps.

In one embodiment of the present invention, the storage capacitor comprises coupling capacitances of metals. According to one embodiment of the invention, an inner electrode and an outer electrode of the storage capacitor are constructed from stacks enclosing metal pieces and the contact elements connecting these metal pieces. In addition, according to one embodiment of the invention several outer electrodes are grouped around an inner electrode in order to maximise the capacity for the storage capacitor and to guarante screening from the adjacent storage capacitors or memory cells.

In a memory cell arrangement, several storage capacitors according to one embodiment of the invention of uniform shape can be arranged next to one another, with joint use being made of the outer electrodes of the adjacent storage capacitors. For production considerations and because of the better screening from adjacent storage capacitors a hexagonal shape is used in one embodiment. All outer electrodes of the memory cell arrangement can be connected together with a further metal part that is applied to a reference potential or a supply voltage.

One embodiment of the present invention is suited to use in microelectronic circuits in order, for example in system-on-chip applications, to create 1T-, 2T- or 3T-memory cells. The invention is obviously not restricted to this area of application, however.

Brief Description of the Drawings

The accompanying drawings are included to provide a further understanding of the present invention and are incorporated in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain the principles of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated as they become better understood by reference to the following detailed

description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

Figure 1 illustrates a side view of a storage capacitor according to a preferred embodiment of the invention.

Figure 2 illustrates a top view of a storage capacitor according to the invention.

Figures 3A-3C illustrate examples of even arrangements of outer (second) electrodes and inner (first) electrodes in storage capacitors according to the invention.

Figures 4A and 4B illustrate examples of connections between the outer electrodes of adjacent storage capacitors.

Figures 5A-5C illustrate examples of the control of a storage capacitor according to the invention by means of 1T-, 2T- and 3T-memory cells.

Detailed Description

Figure 1 illustrates a side view of a storage capacitor with an inner (first) electrode 1 in the center, two adjacent outer (second) electrodes 2 and a metal part 3 connecting the outer electrodes.

In a manner according to one embodiment of the invention, lateral capacities between adjacent conductors are used to construct the storage capacitor. A stack of metal parts 5 and contact elements 6 connecting these metal parts 5 is constructed, in order to form the corresponding electrode 1 or 2 of the storage capacitor, as illustrated in Figure 1. Between a stack and an adjacent stack the desired memory capacity is then created, with the two stacks being arranged in parallel.

When used in microelectronic circuits the metal parts 5 are so-called landing-pads and are each positioned in a metal layer 4. The contact elements 6 connecting the metal parts 5 are so-called vias and are positioned between the metal layers 4.

Advantages of this solution compared with the normal design of a storage capacitor in microelectronic circuits include the reduction in leakage currents within the memory capacity itself, by avoiding MOS or diffusion capacitances, and simple implementation by means of standard metallization in a purely standard CMOS process.

In order to maximise the memory capacity and to guarantee screening from adjacent storage capacitors, several outer electrodes 2 are arranged around an inner electrode 1, as illustrated by way of example in Figure 2.

Figure 2 illustrates a top view of a storage capacitor according to one embodiment of the invention without metal part with an inner electrode 1 in the centre and four adjacent outer electrodes 2 in the shape of a diamond, indicating the lateral memory capacities between the outer electrodes 2 and the inner electrode 1.

The outer electrodes 2 are connected via contact elements with a metal part 3, which is applied to a reference potential or a supply voltage (see Figure 1). The inner electrode is coupled with a selection circuit (e.g. a selection transistor) via a contact element.

Several of the storage capacitors described above can be arranged alongside one another to form a memory cell arrangement, with joint use of the outer electrodes being made by the adjacent storage capacitors.

It is possible to assign a storage capacitor not just one inner electrode, but several, which are then connected in parallel by means of separate connections, in order to thereby increase the capacity of the storage capacitor. However, the principle according to one embodiment of the invention can be put into practice by just one inner (first) electrode and one outer (second) electrode, each with a stack-like construction as described.

The outer electrodes of a storage capacitor can be arranged in various forms around the corresponding inner electrode. Since in microelectronic circuits as a rule the metal landing-pads are used as a basis for the construction of the stacks described above, a rectangular shape, a diamond shape and a hexagonal shape are the most advantageous shapes. Figures 3A-3C illustrates these three most advantageous shapes for an even arrangement of the outer electrodes 2 around inner electrodes 1 in a memory cell arrangement according to the invention.

The three shapes illustrated in Figures 3A-3C differ essentially by the space used. Taking the side length of a landing pad as a reference length A and also selecting the same distance between two adjacent landing-pads, then the necessary relative area for the rectangular shape (Fig. 3A) comes to $16A^2$, the relative area for the hexagonal shape (Fig. 3B) comes to $12A^2$ and the relative area for the diamond shape (Fig. 3C) comes to $8A^2$.

Because it is easier lithographically and can be created with a higher yield, the hexagonal shape, which in its three-dimensional form looks like a honeycomb, is preferred for production considerations over the other two shapes. In addition, the screening from the adjacent cells is better with the hexagonal shape than with the other shapes.

Through further connections of the outer electrodes, as illustrated for example in Figures 4A and 4B, the capacity of a storage capacitor can be further increased. Here, the connection between adjacent outer electrodes 2 within a storage capacitor can be achieved both in just one of the metal layers 4 and also in several or all metal layers 4. The same applies to a possible connection between storage capacitors arranged adjacently between outer electrodes 2. It is likewise also in principle conceivable to connect in this way several inner electrodes 1 of a storage capacitor.

In microelectronic circuits through the connection of two adjacent outer electrodes, in Figures 4A and 4B, respectively vertical or horizontal, in each metal layer the storage capacity of the rectangular shape is increased without loss of surface area (see Figure 4A). Likewise, by connecting two outer, each horizontal, electrodes in each metal layer the memory capacity in the hexagonal shape is increased without loss of surface area (see Figure 4B). Furthermore, the hexagonal shape has lower surface area usage than the rectangle.

Figures 5A-5C illustrate possible applications of a storage capacitor 7 according to the invention in 1T-, 2T- and 3T-semiconductor memories or corresponding memory cell arrangements.

According to Figure 5A, the storage capacitor 7 is controlled via its inner electrodes via a selection transistor 10, which in turn is addressed via a bit line 8 and a word line 9. Furthermore, the outer electrodes of the storage capacitor 7 are connected with a reference potential Vref (1T-memory cell concept).

According to Figure 5B, the storage capacitor is controlled via two selection transistors 10a, 10b. Selection transistor 10a is addressed via a first bit line 8a and a first word line 9a, while selection transistor 10b is addressed via a second bit line 8b and a second word line 9b (2T-memory cell concept). The storage capacitor 7 is connected via its

inner electrodes with the two selection transistors 10a, 10b, while the outer electrodes are again applied to the reference potential Vref.

According to Figure 5C, three transistors 10a, 10b and 10c are used, which are connected to the storage capacitor 7 as shown. The first bit line 8a and first word line 9a assigned to selection transistor 10a serve to write or store information in the storage capacitor 7, which is applied to a first reference potential Vref1. The second bit line 8b and second word line 9b assigned to selection transistor 10c serve to read out the information stored in the storage capacitor. The transistor 10b connecting the storage capacitor 7 with the selection transistor 10c is applied to a second reference potential Vref2 (3T-memory cell concept).

Of course, the connections of the inner and outer electrodes of the storage capacitor to the selection transistor(s) and the reference potential (or the supply potential) can also be swapped over.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.

STORAGE CAPACITOR WITH HIGH MEMORY CAPACITY AND LOW SURFACE AREA

Cross-Reference to Related Applications

This Utility Patent Application claims priority to German Patent Application No. DE 103 03 738.1, filed on January 30, 2003, which is incorporated herein by reference.

~~FIELD OF THE INVENTION~~Background

The present invention relates to a storage capacitor, in particular one that can be used for 1T-, 2T- and 3T-memory cells in, for example, system-on-chip applications, which provides ~~the highest possible~~high capacity with low surface area usage.

~~BACKGROUND OF THE INVENTION~~

In dynamic RAM memories, the information to be stored by a memory cell is generally held on a capacitor known as a storage capacitor. In system-on-chip applications in a pure logic technology, storage capacitors are often created by means of the gate capacity of an MOS transistor (e.g. a MoSyS-1T-SRAM, a 1T-cell of a static random access memory from MoSys Inc.) or by means of connection in parallel of gate and diffusion capacity (e.g. IFX-2T concept, a 2T-cell concept from Infineon).

Because of the leakage currents, a storage capacitor slowly loses its charge, which can lead to the loss of the information stored on the capacitor. In order to counter this, in microelectronic circuits the charge of all storage capacitors is refreshed again at certain intervals, so that the information is retained. This interval depends, amongst other things, on the size of the memory capacity.

As a result of increasing integration, the leakage currents in the abovementioned system-on-chip applications are becoming ever greater and new leakage current sources such as the gate leakage currents are arising due to the increasingly thin oxide coatings. The total memory capacity is also becoming smaller.

Summary

~~An object~~One embodiment of the invention ~~is to~~ provides a storage capacitor with high~~the highest possible~~ memory capacity ~~and the lowest possible~~low surface area usage, which in particular in a pure logic technology can be created without additional, and thus more expensive, process steps.

~~SUMMARY OF THE INVENTION~~

~~Within the context~~In one embodiment of the present invention, the storage capacitor comprises coupling capacitances of metals. ~~Here, a~~According to one embodiment of the invention, an inner electrode and an outer electrode of the storage capacitor are constructed from stacks enclosing metal pieces and the contact elements connecting these metal pieces. In addition, according to one embodiment of the invention several outer electrodes are grouped around an inner electrode~~,~~ in order to maximise the capacity for the storage capacitor and to guarantee screening from the adjacent storage capacitors or memory cells.

In a memory cell arrangement, several storage capacitors according to one embodiment of the invention of uniform shape can be arranged next to one another, with joint use being made of the outer electrodes of the adjacent storage capacitors. For production considerations and because of the better screening from adjacent storage capacitors a hexagonal shape ~~is preferred here~~is used in one embodiment. All outer electrodes of the memory cell arrangement can be connected together with a further metal part that is applied to a reference potential or a supply voltage.

One embodiment of ~~T~~the present invention is ~~preferably~~ suited to use in microelectronic circuits in order, for example in system-on-chip applications, to create 1T-, 2T- or 3T-memory cells. The invention is obviously not restricted to this ~~preferred~~ area of application, however.

Brief Description of the Drawings

The accompanying drawings are included to provide a further understanding of the present invention and are incorporated in and constitute a part of this specification. The drawings illustrate the embodiments of the present invention and together with the description serve to explain the principles of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated as they become better understood by reference to the following detailed description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

~~The present invention will now be explained in more detail with reference to the attached drawing and using preferred embodiments.~~

~~Fig.~~Figure 1 ~~shows~~illustrates a side view of a storage capacitor according to a preferred embodiment of the invention.

~~Fig.~~Figure 2 ~~shows~~illustrates a top view of a storage capacitor according to the invention.

~~Figs.~~Figures 3A-3C ~~show~~illustrate examples of even arrangements of outer (second) electrodes and inner (first) electrodes in storage capacitors according to the invention.

~~Figs.~~Figures 4A and 4B ~~show~~illustrate examples of connections between the outer electrodes of adjacent storage capacitors.

~~Figs.~~Figures 5A-5C ~~show~~illustrate examples of the control of a storage capacitor according to the invention by means of 1T-, 2T- and 3T-memory cells.

Detailed Description

~~Fig.~~Figure 1 ~~shows~~illustrates a side view of a storage capacitor with an inner (first) electrode 1 in the cent~~re~~er, two adjacent outer (second) electrodes 2 and a metal part 3 connecting the outer electrodes.

In a manner according to one embodiment of the invention, lateral capacities between adjacent conductors are used to construct the storage capacitor. ~~For this purpose, in each case a~~A stack of metal parts 5 and contact elements 6 connecting these metal parts 5 is constructed, in order to form the corresponding electrode 1 or 2 of the storage capacitor, as ~~shown~~illustrated in ~~Fig.~~Figure 1. Between a stack and an adjacent stack the desired memory capacity is then created, with the two stacks ~~in particular~~ being arranged in parallel.

When used in microelectronic circuits the metal parts 5 are so-called landing-pads and are each positioned in a metal layer 4. The contact elements 6 connecting the metal parts 5 are so-called vias and are positioned between the metal layers 4.

Advantages of this solution compared with the normal design of a storage capacitor in microelectronic circuits include the reduction in leakage currents within the memory capacity itself, by avoiding MOS or diffusion capacitances, and simple implementation by means of standard metallization in a purely standard CMOS process.

In order to maximise the memory capacity and to guarantee screening from adjacent storage capacitors, several outer electrodes 2 are arranged around an inner electrode 1, as ~~shown~~illustrated by way of example in ~~Fig.~~Figure 2.

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The outer electrodes 2 are connected via contact elements with a metal part 3, which is applied to a reference potential or a supply voltage (see ~~Fig.~~Figure 1). The inner electrode is coupled with a selection circuit (e.g. a selection transistor) via a contact element.

Several of the storage capacitors described above can be arranged alongside one another to form a memory cell arrangement, with joint use of the outer electrodes being made by the adjacent storage capacitors.

It is~~, furthermore,~~ possible to assign a storage capacitor not just one inner electrode, but several, which are then connected in parallel by means of separate connections, in order to thereby increase the capacity of the storage capacitor. ~~Essentially, h~~However, the principle according to one embodiment of the invention can be put into practice by just one inner (first) electrode and one outer (second) electrode, each with a stack-like construction as described.

The outer electrodes of a storage capacitor can be arranged in various forms around the corresponding inner electrode. Since in microelectronic circuits as a rule the metal landing-pads are used as a basis for the construction of the stacks described above, a rectangular shape, a diamond shape and a hexagonal shape are the most advantageous shapes. ~~Figs.~~Figures 3A-3C ~~show~~ illustrates these three most advantageous shapes for an even arrangement of the outer electrodes 2 around inner electrodes 1 in a memory cell arrangement according to the invention.

The three shapes ~~shown~~illustrated in ~~Figs.~~Figures 3A-3C differ essentially by the space used. Taking the side length of a landing pad as a reference length A and also selecting the same distance between two adjacent landing-pads, then the necessary relative area for the rectangular shape (Fig. 3A) comes to $16A^2$, the relative area for the hexagonal shape (Fig. 3B) comes to $12A^2$ and the relative area for the diamond shape (Fig. 3C) comes to $8A^2$. Because it is easier lithographically and can be created with a higher yield, the hexagonal shape, which in its three-dimensional form looks like a honeycomb, is preferred for production considerations over the other two shapes. In addition, the screening from the adjacent cells is better with the hexagonal shape than with the other shapes.

Through further connections of the outer electrodes, as ~~shown~~illustrated for example in ~~Figs.~~Figures 4A and 4B, the capacity of a storage capacitor can be further increased. Here, the connection between adjacent outer electrodes 2 within a storage capacitor can be achieved both in just one of the metal layers 4 and also in several or all metal layers 4. The same applies to a possible connection between storage capacitors

arranged adjacently between outer electrodes 2. It is likewise also in principle conceivable to connect in this way several inner electrodes 1 of a storage capacitor.

In microelectronic circuits through the connection of two adjacent outer electrodes, in ~~Figs.~~Figures 4A and 4B, respectively vertical or horizontal, in each metal layer the storage capacity of the rectangular shape is increased without loss of surface area (see ~~Fig.~~Figure 4A). Likewise, by connecting two outer, each horizontal, electrodes in each metal layer the memory capacity in the hexagonal shape is increased without loss of surface area (see ~~Fig.~~Figure 4B). Furthermore, the hexagonal shape has lower surface area usage than the rectangle.

~~Figs.~~Figures 5A-5C ~~shows~~illustrate possible applications of a storage capacitor 7 according to the invention in 1T-, 2T- and 3T-semiconductor memories or corresponding memory cell arrangements.

According to ~~Fig.~~Figure 5A, the storage capacitor 7 is controlled via its inner electrodes via a selection transistor 10, which in turn is addressed via a bit line 8 and a word line 9. Furthermore, the outer electrodes of the storage capacitor 7 are connected with a reference potential Vref (1T-memory cell concept).

According to ~~Fig.~~Figure 5B, the storage capacitor is controlled via two selection transistors 10a, 10b. Selection transistor 10a is addressed via a first bit line 8a and a first word line 9a, while selection transistor 10b is addressed via a second bit line 8b and a second word line 9b (2T-memory cell concept). The storage capacitor 7 is connected via its inner electrodes with the two selection transistors 10a, 10b, while the outer electrodes are again applied to the reference potential Vref.

According to ~~Fig.~~Figure 5C, three transistors 10a, 10b and 10c are used, which are connected to the storage capacitor 7 as shown. The first bit line 8a and first word line 9a assigned to selection transistor 10a serve to write or store information in the storage capacitor 7, which is applied to a first reference potential Vref1. The second bit line 8b and second word line 9b assigned to selection transistor 10c serve to read out the information stored in the storage capacitor. The transistor 10b connecting the storage capacitor 7 with the selection transistor 10c is applied to a second reference potential Vref2 (3T-memory cell concept).

Of course, the connections of the inner and outer electrodes of the storage capacitor to the selection transistor(s) and the reference potential (or the supply potential) can also be swapped over.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.